WHAT IS CLAIMED IS:

1. A phase-changeable memory device, comprising:

a substrate;

an access transistor formed in and/or on the substrate;

laterally spaced apart first and second conductive patterns disposed on the substrate and having opposing sidewalls;

a conductor electrically connecting the first conductive pattern to a source/drain region of the access transistor; and

a phase-changeable material region disposed between the first and second conductive patterns and contacting the opposing sidewalls of the first and second conductive patterns.

2. A memory device according to Claim 1:

wherein the access transistor comprises:

first and second source/drain regions in the substrate; and

a gate electrode disposed on the substrate between the first and second source drain regions;

wherein the memory device further comprises an insulating layer disposed on the substrate and overlying the gate electrode and the first and second source/drain regions;

wherein the first and second conductive patterns are disposed on the insulating layer;

wherein the conductor passes through the insulating layer and connects the first conductive pattern to the first source/drain region; and

wherein the phase-changeable material layer is disposed on the insulating layer between the first and second conductive patterns.

3. A memory device according to Claim 2, wherein the first and second conductive patterns overlie respective ones of the first and second source/drain regions, and wherein the phase-changeable material region overlies the gate electrode.

4. A memory device according to Claim 3, wherein the conductor extends from the first source/drain region to contact the overlying first conductive pattern at a first contact area, and wherein the first conductive pattern contacts the phase-

changeable material region at a second contact area that is substantially smaller than the first contact area.

5. A memory device according to Claim 4:

wherein the insulating layer comprises a first insulating layer;

wherein the conductor comprises a first conductor, and wherein the memory device further comprises:

a second insulating layer disposed on the substrate and overlying the first and second conductive patterns; and

a second conductor passing through the second insulating layer and contacting the second conductive pattern at a third contact area; and

wherein the second conductive pattern contacts the phase-changeable material region at a fourth contact area that is substantially smaller than the third contact area.

6. A memory device according to Claim 5, wherein each of the first and second conductive patterns comprises a body portion that contacts the corresponding one of the first and second conductors and a smaller tab portion that extends from the body portion to contact the phase-changeable material region.

7. A memory device according to Claim 5, further comprising:

a bit line conductor disposed on the second insulating layer, wherein the second conductor electrically connects the second conductive pattern to the bit line conductor;

a common drain line conductor disposed in the first insulating layer between the second conductive pattern and the second source/drain region; and

a third conductor extending from the second source/drain region to contact the common drain line conductor.

8. A memory device according to Claim 1, wherein the phase-changeable material layer comprises a material having a resistivity that is dependent upon a phase of the phase-changeable material region.

9. A memory device according to Claim 8, wherein the phase-changeable material layer comprises a compound of germanium (Ge), stibium (Sb) and tellurium (Te).

10. A phase-changeable memory cell, comprising:

first and second spaced apart conductive patterns having opposing sidewalls; and

a phase-changeable material region disposed between the first and second conductive patterns and contacting the opposing sidewalls thereof.

11. A memory cell according to Claim 1, wherein each of the first and second conductive patterns comprise:

a body portion configured to contact a conductor at a first contact area;

a tab portion extending from the body portion to contact the phase-changeable material region at a second contact area that is perpendicular to the first contact area and that is substantially smaller than the first contact area.

12. A phase-changeable memory device structure comprising:

a pair of conductive patterns spaced apart from each other on the same plane;

a variable resistor pattern disposed between the pair of conductive patterns so as to be in direct contact with opposing sidewalls of the conductive patterns at active contact areas;

an upper metal interconnection disposed over the conductive patterns and the variable resistor pattern, wherein the upper metal interconnection is electrically connected to one conductive pattern; and

a semiconductor substrate disposed below the conductive patterns and the variable resistor pattern, wherein the semiconductor substrate has an impurity diffusion region that is electrically connected to the other conductive pattern.

13. The structure as claimed in claim 12, wherein the variable resistor pattern includes a phase-changeable material.

14. The structure as claimed in claim 12, wherein the upper metal interconnection is electrically connected to one conductive pattern through an upper

contact plug penetrating an upper insulating layer disposed on the conductive patterns and the variable resistor pattern,

wherein the impurity diffusion region is electrically connected to the other conductive pattern through a lower contact plug penetrating a lower insulating layer disposed under the conductive patterns and the variable resistor pattern.

15. The structure as claimed in claim 14, further comprising:

another impurity diffusion region spaced apart from the impurity diffusion region in the semiconductor substrate;

a gate line disposed on a semiconductor substrate between the impurity diffusion region and the other impurity diffusion region, and in the lower insulating layer; and

a common drain electrode disposed in the lower insulating layer, wherein the common drain electrode is electrically connected to the other impurity diffusion region through a predetermined region of the lower insulating layer.

16. The structure as claimed in claim 12, wherein a crystallization structure of a variable resistor material constituting the active contact areas is changed depending on density of currents flowing across the active contact area of the variable resistor pattern.

17. The structure as claimed in claim 15, wherein when current flows between the upper metal interconnection and the common drain electrode a crystallization structure of a variable resistor material constituting the active contact areas is changed depending on density of currents flowing across the active contact area of the variable resistor pattern.

18. The structure as claimed in claim 12, wherein the pair of conductive patterns includes titanium nitride.

19. The structure as claimed in claim 12, wherein the lower contact plug and the upper contact plug include respectively titanium, titanium nitride, and tungsten that are sequentially stacked.

20. A phase-changeable memory device structure comprising:

a phase-changeable material pattern having active contact areas at both sides thereof;

a pair of conductive patterns disposed symmetrically on the same plane as the phase-changeable material pattern, wherein the conductive patterns are in direct contact with the active contact areas of the phase-changeable material pattern;

an upper insulating layer disposed on the phase-changeable material pattern and the conductive patterns;

a bit line disposed on the upper insulating layer, wherein the bit line is electrically connected to one conductive pattern through an upper contact plug penetrating the upper insulating layer;

a lower insulating layer disposed under the phase-changeable material pattern and the conductive patterns; and

a semiconductor substrate having a source region electrically connected to the other conductive pattern through a lower contact plug penetrating the lower insulating layer.

21. The structure as claimed in claim 20, further comprising:

a drain region spaced apart from the source region to be formed in the semiconductor substrate;

a gate line disposed on a semiconductor substrate between the source and drain regions; and

a common drain electrode disposed in the lower insulating layer, wherein the common drain electrode is electrically connected to the drain region through a predetermined region of the lower insulating layer.

22. The structure as claimed in claim 20, wherein the conductive pattern includes titanium nitride.

23. The structure as claimed in claim 21, wherein a crystallization structure of a phase-changeable material constituting the active contact areas is changed depending on density of currents flowing across the active contact areas of the variable resistor pattern, so that resistivity of the active contact areas is varied.

24. A phase-changeable memory device structure comprising:

a phase-changeable material pattern having active contact areas at both sides thereof;

a first electrode pattern disposed on the same plane as the phase-changeable material pattern, wherein the first electrode pattern is in contact with one active contact area;

a second electrode pattern disposed on the same plane as the phase-changeable material pattern, wherein the second electrode pattern is in contact with the other active contact area;

a resistance detection interconnection electrically connected to the second electrode interconnection; and

a semiconductor substrate including an impurity diffusion region electrically connected to the first electrode interconnection.

25. The structure as claimed in claim 24, wherein an upper insulating layer is interposed between the phase-changeable material pattern and the resistance detection interconnection and between the electrode patterns and the resistance detection interconnection, and the resistance detection interconnection is electrically connected to the second electrode pattern through an upper contact plug penetrating the upper insulating layer,

wherein a lower insulating layer is interposed between the phase-changeable material pattern and the semiconductor substrate and between the electrode patterns and the semiconductor substrate, and the impurity diffusion region is electrically connected to the first electrode pattern through a lower contact plug penetrating the lower insulating layer.

26. The structure as claimed in claim 25, wherein each electrode pattern includes a plug contact region contacting with a contact plug and a material pattern contact region protruding from a middle portion of sidewalls of the plug contact region toward the phase-changeable material pattern to be in contact with the active contact area.

27. The structure as claimed in claim 26, wherein dimensions of the active contact area is determined according to a thickness and a width of the material pattern contact region.

28. The structure as claimed in claim 27, wherein the width of the material pattern contact region is less than the thickness thereof.

29. A method of forming a phase-changeable memory device, comprising:

forming an access transistor in and/or on a substrate;

forming first and second conductive patterns laterally spaced apart on the substrate and having opposing sidewalls;

forming a conductor electrically connecting the first conductive pattern to a source/drain region of the access transistor; and

forming a phase-changeable material region between the first and second conductive patterns and contacting the opposing sidewalls of the first and second conductive patterns.

30. A method according to Claim 29:

wherein forming an access transistor comprises:

forming a gate electrode on the substrate; and

forming first and second source/drain region outside of the gate electrode;

wherein forming first and second conductive patterns is preceded by:

forming an insulating layer on the first and second source/drain regions and the gate electrode; and

forming the conductor to extend from the first source/drain region through the insulating layer;

wherein forming first and second conductive patterns comprises forming the first and second conductive patterns on the insulating layer overlying respective ones of the first and second source/drain regions such that the first conductive pattern contacts the conductor extending through the insulating layer; and

wherein forming a phase-changeable material region comprises forming the phase-changeable material region on the insulating layer between the first and second conductive patterns.

31. A method according to Claim 30, wherein the conductor contacts the first conductive pattern at a first contact area, and wherein the phase-changeable material region contacts the first conductive pattern at a second contact area that is smaller than the first contact area.

32. A method according to Claim 30, wherein the first conductive pattern has a body portion that contacts the first conductive area and a smaller tab portion that extends from the body portion and contacts the phase-changeable material region.

33. A method according to Claim 30:

wherein forming first and second conductive patterns comprises:

depositing a conductive layer on the insulating layer; and

patterning the conductive layer to form the first and second conductive patterns and to expose a portion of the insulating layer therebetween;

wherein forming a phase-changeable material region is preceded by forming masking regions on the first and second conductive patterns; and

wherein forming a phase-changeable material region comprises:

forming a phase-changeable material layer covering the masking regions and contacting the exposed portion of the insulating layer and sidewalls of the first and second conductive patterns; and

removing portions of the phase-changeable material layer to leave the phase-changeable material region disposed on the exposed portion of the insulating layer and contacting the sidewalls of the first and second conductive patterns.

34. A method according to Claim 33, wherein patterning the conductive layer comprises:

removing portions of the conductive layer to leave a conductive pattern extending over the first and second source/drain regions and the gate electrode;

forming a masking layer on the conductive pattern; and

removing portions of the masking layer and the conductive pattern overlying the gate electrode to form the first and second conductive patterns and to expose the portion of the insulating layer therebetween.

35. A method according to Claim 33, wherein patterning the conductive layer comprises:

forming a masking layer on the conductive layer; and

removing portions of the masking layer and the conductive layer to leave the first and second conductive patterns and respective first and second masking regions on the first and second conductive patterns and to expose a the portion of the insulating layer therebetween.

36. A method according to Claim 30:

wherein forming a phase-changeable material region comprises:

forming a phase-changeable material layer on the insulating layer;

forming a masking layer on the phase-changeable material layer; and

patterning the phase-changeable material layer and the masking layer to form the phase-changeable material region and a masking region on the phase-changeable material region;

wherein forming the first and second conductive patterns comprises:

forming a conductive layer covering the masking layer and adjacent portions of the insulating layer and contacting sidewalls of the phase-changeable material layer; and

removing portions of the conductive layer and the masking layer to form the first and second conductive patterns and to expose a portion of the phase-changeable material region between the first and second conductive patterns.

37. A method according to Claim 30, wherein the conductor comprises a first conductor, wherein the insulating layer comprises a first insulating layer, and further comprising:

forming a second insulating layer on the first and second conductive patterns;

forming a second conductor extending from the second conductive pattern through the second insulating layer.

38. A method according to Claim 37, wherein the second conductor contacts the second conductive pattern at a first contact area, and wherein the phase-

changeable material region contacts the second conductive pattern at a second contact area that is smaller than the first contact area.

39. A method according to Claim 37, wherein the second conductive pattern comprises a body portion that contacts the second conductor and a smaller tab portion extending from the body portion to contact the phase-changeable material region.

40. A method according to Claim 37, further comprising forming a bit line on the second insulating layer and contacting the second conductor.

41. A method according to Claim 30:

wherein forming an insulating layer comprises forming a first insulating layer on the first and second source/drain regions and the gate electrode;

wherein forming a conductor comprises:

forming a first conductive plug contacting the first source/drain region and passing through the first insulating layer; and

forming a conductive pad on the first insulating layer and contacting the first conductive plug;

wherein forming an insulating layer further comprises forming a second insulating layer on the first insulating layer;

wherein forming a conductor further comprises forming a second conductive plug contacting the conductive pad and extending through the second conductive layer; and

wherein forming first and second conductive patterns comprises forming the first and second conductive patterns on the second insulating layer.

42. A method according to Claim 41, further comprising:

forming a third conductive plug contacting the second source/drain region and passing through the first insulating layer; and

forming a common drain line contact pad on the first insulating layer and contacting the third conductive plug.

43. A method of forming a memory device comprising:

providing a semiconductor substrate having an impurity diffusion region;

forming a conductive layer that is electrically connected to the impurity diffusion region;

patterning the conductive layer to form a symmetrical pair of conductive patterns so that one conductive pattern is electrically connected to the impurity diffusion region;

forming a variable resistor pattern between the pair of conductive patterns, wherein the variable resistor pattern includes active contact areas that is in direct contact with opposite sidewalls of the conductive patterns; and

forming a metal interconnection that is electrically connected to the other conductive pattern.

44. A method of forming a phase-changeable memory device comprising:

forming a source region, a drain region, and a gate electrode on a semiconductor substrate;

forming a common drain electrode to be isolated from the semiconductor substrate by an insulating layer and to be electrically connected to the drain region through a predetermined region of the insulating layer;

forming a lower insulating layer on the resultant structure where the common drain electrode is formed;

forming a lower contact plug in the lower insulating layer to be electrically connected to the source region;

sequentially forming a phase-changeable material layer and a protective insulating layer on the lower insulating layer and the lower contact plug;

successively patterning the protective insulating layer and the phase-changeable material layer to form a protective insulating pattern and a phase-changeable material pattern so as not to be in contact with the lower contact plug;

forming a conductive layer on the lower insulating layer, the lower contact plug, and the patterns in order to supply currents to the phase-changeable material pattern;

patterning the conductive layer so that an upper portion of the phase-changeable material pattern is partially exposed, to form a pair of conductive patterns such that one conductive pattern is electrically connected to the lower contact plug,

wherein the pair of conductive patterns is apart from each other by the phase-changeable material pattern and is in direct contact with both sidewalls of the phase-changeable material pattern;

forming an upper insulating layer on the lower insulating layer, the conductive patterns and the exposed phase-changeable material pattern;

forming an upper contact plug electrically connected to the other conductive pattern that is not electrically connected to the lower contact plug; and

forming a metal interconnection on the upper insulating layer to be electrically connected to the upper contact plug.

45. A method of forming a phase-changeable memory device comprising:

forming a source region, a drain region, and a gate electrode at a semiconductor substrate;

forming a common drain electrode to be electrically isolated from the other regions of the semiconductor substrate excepting the drain region and to be electrically connected to the drain region;

forming a lower insulating layer on the resultant structure where the common drain electrode is formed;

forming a lower contact plug in the lower insulating layer to be electrically connected to the source region;

forming a conductive layer on the lower insulating layer and the lower contact plug;

patterning the conductive layer to form a symmetrical pair of conductive patterns apart from each other so that one conductive pattern is in contact with the lower contact plug;

forming a chalcogenide material pattern between the pair of conductive patterns so as to be in direct contact with opposite sidewalls of the pair of conductive patterns;

forming an upper insulating layer on the resultant structure where the material pattern is formed;

forming an upper contact plug electrically connected to the other conductive pattern that is not electrically connected to the lower contact plug; and

forming a metal interconnection on the upper insulating layer to be electrically connected to the upper contact plug.